REMARKS

Claims 1-16 are now present in connection with the present application. Claims 1, 10, 13 and 15 are the sole remaining independent claims.

Objection to the Specification

The Examiner has objected to the Specification because of minor informalities and because of spacing requirements. Applicants have corrected the minor informalities and submit herewith a Substitute Specification including paragraph numbers as desired by the United States Patent and Trademark Office. Proper spacing is believed to be present throughout the Substitute Specification.

Further with regard to the Examiner's objection, the alleged informality appears to be a typographical error. Thus, the Specification has been amended to change "from a CPU to and LSI" to --from a CPU to an LSI--. Support for this amendment can be found on at least original application page 11, lines 12-13, wherein the Specification recites "from a CPU (host system) to an LSI (peripheral device)".

Accordingly, entry of the Substitute Specification and withdrawal of the Examiner's objection is respectfully requested.

Claim Objections

The Examiner has objected to claims 8, 13 and 15 because of minor informalities, alleging that proper spacing is not present throughout the claims. Accordingly, the claims have been represented in the present Amendment, noting that no actual amendments have been made to the claims. The claims are believed to include proper spacing and thus have each been represented with the identifiers

"Previously Presented", as no substantive changes to the claims have been made.

Withdrawal of the objection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 112

The Examiner has rejected claim 3 under 35 U.S.C. § 112, first paragraph, alleging that it fails to comply with the enabling requirement. The Examiner has alleged that the claim contains subject matter which is not described in the Specification in such a way to enable one of ordinary skill in the art to which it pertains, or which is most nearly connected, to make and use the invention. This rejection is respectfully traversed.

Specifically, the Examiner's objection focuses on the perceived differences between independent claim 1 and dependent claim 3. The Examiner alleges that the preamble of claim 1 states that a first device divides the data into data group. The Examiner alleges that the first device is the LSI according to the Specification (pointing to figure 1B, and page 11, first paragraph of the Specification). The Examiner then alleges that claim 3 recites that the division pattern is in accordance with an instruction from the first device, alleging that the number of divisions is based on the CPU's instructions (pointing to page 3, last paragraph of the Specification). Accordingly, it appears that the Examiner's main issue, therefore, is that the first device in claim 1 corresponds to the LSI, and the same first device in claim 3 corresponds to the CPU. This assertion is also traversed.

A somewhat similar rejection has been made with regard to claim 8, wherein the Examiner alleges that the first device in claim corresponds to the LSI, and the first device in claim 8 corresponds to a CPU. This assertion is also traversed.

With respect to both rejection of claims 3 and 8, the Examiner's understanding of the present application is not correct. Thus, Applicants respectfully traverse the Examiner's rejection for at least the following reasons.

Initially, it appears that the Examiner is referring to different embodiments of the present application to support rejections of each of claims 3 and 8. This understanding is incorrect, as will be explained as follows.

Claim 1 recites "a data bus width conversion apparatus for receiving N-bit data (N is a positive integer) from a first device having a first bus width (this is supported by, but not limited to, page 14, lines 13-14 of the original application for example) and outputting the N-bit data to a second device having a second bus width, wherein the first device divides the N-bit data into a plurality of bit data groups and the plurality of bit data groups are transferred to the apparatus (supported by, but necessarily limited to page 10, lines 15-19 of the present application).

In particular, the supporting Specification clearly recites "**a CPU** (host system) **divides N-bit data** (N is a positive integer) into plurality of bit data groups, and division patterns of the N-bit data for dividing the N-bit data into a plurality of bit data groups" (emphasis added) (again supported by, but not necessarily limited to page 10, lines 15-19 of the present application). **Therefore, the Examiner's assertion that the first device must be the LSI is clearly improper**. The first device may be the CPU.

Accordingly, claim 3 is fully enabled, wherein it states that the division pattern is in accordance with instruction from the first device (supported by, but not necessarily limited to **CPU 10** of the present application). As such, both claims 1 and 3 are clearly consistent with one another based on such an interpretation. Thus, withdrawal of the Examiner's rejection of claim 3 is requested.

Similarly, claim 8 is also fully enabled. Claim 8

calls for the apparatus outputting the N-bit data to the second device and a data write access from the first device (supported by, but not necessarily limited to CPU 10) to the second device. Thus, withdrawal of the Examiner's rejection of claim 8 is requested.

Accordingly, both claims 3 and 8 are fully enabled by the present Specification and Applicants further submit that such an interpretation of claims 1 and 3 and claims 1 and 8 is also clearly consistent with and fully supported by an enabling Specification. Accordingly, withdrawal of the Examiner's rejection of claims 3 and 8 under 35 U.S.C. § 112, first paragraph is respectfully requested.

Prior Art Rejections

The Examiner has rejected claims 1-2, 4, 7 and 9-16 under 35 U.S.C. § 102 as being anticipated by Applicants admitted prior art. This rejection is respectfully traversed.

Claim 1 of the present application is directed to a data bus width conversion apparatus, comprising at least "a setting section for setting the total number of transferred options …, and for setting a division pattern of the N-bit data …". At least such a limitation is not taught or suggested by Applicants admitted prior art, **which includes no such setting section**.

The Examiner asserts that Applicants admitted prior art discloses dividing the LSIs bus width to accommodate the CPUs instruction and dividing the 18-bit information at least three times with various division patterns. The Examiner alleges that this aspect of Applicants admitted prior art meets the aforementioned "setting section" of claim 1. Applicants respectfully disagree with the Examiner's assertion.

Applicants admitted prior art instead merely discloses

an example whereby, in the case of a liquid crystal module having a data bus width of 18 bits being connected to a CPU data bus width of 8 bits, is necessary to divide the 18 bits of data into at least three portions so as to transfer the data from the CPU to the liquid crystal molecule. The Examiner alleges that there are various division patterns, but illustrates no "setting section" as claimed..

Applicants admitted prior art fails to disclose at least such a "setting section" as set forth in claim 1. In particular, Applicants admitted prior art specifically states that the **number of axis operations** by the CPU required for transfer of N-bit data from the CPU to an LSI, and the division pattern, **are fixed in hardware** (see page 2, lines 11-18 and page 4, lines 1-8 of the original application Specification). Thus, since the division pattern and the number of divisions of the 18-bit data are **fixed in hardware**, it is **unnecessary and redundant to have a setting section** for setting the total number of transfer operations and for setting a division pattern as disclosed in claim 1 for example. Thus, Applicants admitted prior art fails to teach or suggest at least such a feature. Accordingly, withdrawal of the rejection is requested.

Further, the setting section as disclosed in claim 1 has the advantage that the number of divisions and the division pattern can be arbitrarily set (see page 11, lines 9-14 of the present application). Accordingly, Applicants admitted prior art is clearly missing such a limitation and thus cannot achieve such an advantage.

As provided in MPEP § 2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference". *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Stated another way, "the identical invention must be shown in as complete detail as is contained in

the…claims". *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In deciding the issue of anticipation, the trier of fact must identify the elements of the claims, determine their meaning in light of the Specification and Prosecution history, and identify corresponding elements disclosed in the allegedly anticipating references (emphasis added, citations in support omitted).

Therefore, Applicants respectfully submit that Applicants admitted prior art fails to disclose at least a setting section as set forth in claim 1, and thus Applicants admitted prior art is clearly missing at least one element of claim 1 and thus cannot be held to anticipate claim 1. Further, there is nothing in Applicants prior art that would also teach or suggest or render such a limitation obvious, let alone teach or suggest the associated advantages. Accordingly, withdrawal of the Examiner's rejection is respectfully requested.

With regard to independent claim 10, this claim is directed to a data bus width conversion apparatus comprising at least "a setting section". Accordingly, as such a setting section is not taught or suggested by Applicants admitted prior art, Applicants respectfully submit that claim 10 is allowable for at least reasons somewhat similar to those previously set forth with regard to independent claim 1. Accordingly, withdrawal of the Examiner's rejection of claim 10 is respectfully requested.

With regard to claim 13, independent claim 13 is directed to a data processing apparatus comprising a data bus width conversion apparatus. The data bus width conversion apparatus comprises, among other features, a setting section. Accordingly, claim 13 is allowable for at least reasons somewhat similar to those previously set forth with regard to independent claim 1. Accordingly, withdrawal of the Examiner's rejection of claim 13 is also respectfully

requested.

Finally, independent claim 15 is directed to a data processing apparatus comprising a data bus width conversion apparatus. The data bus width conversion apparatus includes, among other features, a setting section. Accordingly, Applicants respectfully submit that claim 15 is allowable over Applicants admitted prior art for reasons somewhat similar to those previously set forth with regard to independent claim 1. Accordingly, withdrawal of the Examiner's rejection of independent claim 15 is respectfully requested.

Allowable Subject Matter

Applicants recognize and wish to thank the Examiner for the indication that claims 5 and 6 are objected to as containing allowable subject matter, and would be allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims. As Applicants believe that independent claim 1 is allowable for the reasons previously set forth, these claims have not be rewritten into independent form at this time.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of pending claims 1-16 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or

credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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